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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/798,394	LIU ET AL.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 6-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2,4,6-15 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 8 – 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu (US7047348).

4. As to claim 8, Wu discloses a debug card device, comprising: a PCI interface operable as a connecting interface with a PCI bus (Figure 2, PCI master element 111);

a storage module for storing PCI bus data; and

a data control chip operable to control the access and transmission of PCI bus data, the data control chip including: an access control module for controlling data access according to a control signal (SMB slave controller 112);

a transmission control module for controlling data transmission according to a control signal (SMB slave controller 112);

a data storage module for storing PCI bus data obtained from the debug card (PCI register block 20);

a register for storing an access control command (SMB slave controller 112 comprises said register); and

a host interface operable as an interface with a host (SMBUS interface 114).

5. As to claim 9, Wu discloses the debug card device of claim 8, further being connected to a host via a host interface, wherein the host comprising: a host interface operable as a connecting interface with the debug card (Figure 2 illustrates said interface in element 114, Col. 4, lines 60 – 67);

a data access module operable to control the access of the PCI bus data in the data control chip of the debug card (Figure 2, element 113, Col. 5, lines 29 – 32);

a driving module providing an access control firmware program (Slave controller of Figure 2 comprises said control firmware, COL. 5, lines 1 – 3); and

a data storage module for storing extracted PCI bus data (Figure 2, element 20, COL. 5, lines 25 – 30).

6. As to claim 10, Wu discloses the debug card device, wherein the storage module is a buffer of the debug card (Register block 20 of Figure 2 comprises said function, COL. 5, lines 5 – 10).

7. As to claim 11, Wu discloses the debug card device, wherein the data storage module is a buffer of the data control chip (Data buffer 113 of Figure 2 comprises said buffer).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 – 2,4,7,14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US7047348), in view of Cypress.

10. As to claim 1, Wu discloses A method of accessing PCI bus data via a debug card, comprising Accessing to data of the PCI bus via a PCI interface of the debug card: (Figure 2 illustrates a system comprising a PCI Interface 111 of debug card that interfaces with the PCI bus 10, COL. 5, lines 4 – 12);

storing the data in a buffer of the debug card (PCI Register block 20 comprise said function, COL. 5, lines 1-3);

controlling the access to the data stored in the buffer of debug card by means of a data control chip of the debug card (The controller SMB controller 112 performs said function, COL. 4, line 65 – COL. 5, line 3);

storing the data in a buffer of the data control chip (Figure 2 illustrates said buffer in element , data buffer 113, COL. 5, lines 28 – 32); and

extracting the data stored in the buffer of the data control chip via a host interface of the debug card (Data extraction is enabled by controller, COL. 4, line 65 – COL. 5, line 3).

Wu does not explicitly disclose the step of controlling the access to the data stored in the buffer of debug card comprising: initializing the data control chip;

If the data control chip is in the idle status, setting the data control chip, wherein the setting step further comprises:

Setting a data access mode of the data control chip;

Determining a data access situation of the debug card and performing counting;

Setting an amount of data to be accessed each time; and

Ending the idle status; and If the data control chip is not in the idle status, accessing to the PCI bus data stored in the debug card according to the settings of the data control chip.

However, Cypress teaches: the step of controlling the access to the data stored in the buffer of debug card comprising: initializing the data control chip (Figure 2 illustrates the interface between a device and General Programmable Interface (GPIF), and the configuration sequence that ensues using the GPIFTool utility, page 3;

If the data control chip is in the idle status, setting the data control chip, wherein the setting step further comprises:

Setting a data access mode of the data control chip (The device via the interface is checked to see its idle status, page 3, paragraph 8);

Determining a data access situation of the debug card and performing counting (Peripheral FIFO write example of page 4 illustrates said function, which comprises counting);

Setting an amount of data to be accessed each time (Setting peripheral single write register, page 4); and

Ending the idle status (Routine 1 on page 8 illustrates ending the idle status, page 8); and If the data control chip is not in the idle status, accessing to the PCI bus data stored in the debug card according to the settings of the data control chip (Read transaction as illustrated in routine 2, page 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the interface of Cypress in the system of Wu as Cypress provides a general purpose interface that can be used in many protocols, page 1, paragraph 1. One of ordinary skill in the art would have been motivated to use the interface of Cypress in the system of Wu as Cypress provides a general purpose interface that can be used in many protocols, page 1, paragraph 1.

11. As to claim 2, Wu discloses The method, wherein extracting the data stored in the buffer of the data control chip via a host interface of the debug card further

comprising: transferring the data stored in the buffer of the data control chip to the host (Figure 2 illustrates the data flow between the host interface 114, the controller 112, and the data buffer 113, COL. 5, lines 30-35); and analyzing the data stored in the host (The system analyze the command type, read/write, COL. 3, lines 5-7).

As to claim 4, Wu discloses the method, wherein initializing the data control chip further comprising: performing a synchronization setting of the data control chip and debug card;

setting an operating mode of the data control chip (Status signal performs said function as slave controller engages PCI master, COL. 5, lines 1-3);

selecting a register address in the data control chip and writing an access control code therein (Said function via the SMB interface, COL2., lines 25-30);

setting a data access width of the data control chip (Data command comprises data width, COL. 2, lines 30 – 35); and

clearing the buffer of the debug card (It is well known in the art of clearing the buffer to conserve memory usage).

12. As to claim 7, Wu discloses the method, wherein if the data control chip is not in an idle status, accessing to the PCI bus data according to the settings of the data control chip means accessing to the PCI bus data according to a control code stored in a register of the data control chip (Figure 2 illustrates the interaction with controller and said elements driven by control code, COL.2, lines 30 – 47).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Cypress and in further view of Tsai et al (US6751754) hereinafter Tsai.

15. As to claim 6, Wu as modified by Cypress does not explicitly disclose the method, wherein ending the idle status further comprising preparing to perform a next data access.

However, Tsai discloses the method, wherein ending the idle status further comprising preparing to perform a next data access (Figure 2 illustrates the address 2 progression, COL. 2, lines 60 – 67). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the single step process of Tsai in the system of Wu as it allows real time inspection of the bus progress by elongating the cycle, COL. 1, lines 57 – 67. One of ordinary skill in the art would have been motivated to use the single step process of Tsai in the system of Wu as it allows real time inspection of the bus progress by elongating the cycle, COL. 1, lines 57 – 67)

16. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu in view of Tsai, and in further view of Landry et al (US6732301) hereinafter Landry.

17. As to claims 12 and 13, Wu as modified by Cypress and Tsai does not disclose the debug card device, wherein the host interface is a USB interface.

However, Landry teaches the debug card device, wherein the host interface is a USB interface as illustrated in Figure 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the USB interface of Landry in the system of Wu/Tsai to afford the capability to support the USB bus system, COL. 2, lines 7 – 28. One of ordinary skill in the art would have been motivated to use the USB interface of Landry in the system of Wu/Tsai to afford the capability to support the USB bus system, COL. 2, lines 7 – 28.

As to claim 14, Cypress discloses the method wherein the data control chip is a chip of a model EZ-USBFX2 (Figure 2 illustrates control chip with said interface, page 3).

As to claim 15, Cypress discloses the method, wherein the determination of the data access situation of the debug card enables to evaluate whether the buffer of the debug card is full, which establishes a basis for calculating an accumulation of the data which means the amount of data accessed each time being accumulated into a data amount total, setting the amount of data determines a number of data packets to access it at a next non-idle status, and once the idle status ends, the control chip turns to the non-idle status to perform data accessing (Peripheral FIFO Write routine on page 4 outlines elements of said transaction, page 4).

Response to Arguments

18. Applicant's arguments filed 3/26/2007 have been fully considered but they are not persuasive. With regards to the applicant's argument that prior art does not teach the step of controlling the access to the data stored in the buffer of debug card comprising: initializing the data control chip;

If the data control chip is in the idle status, setting the data control chip, wherein the setting step further comprises:

Setting a data access mode of the data control chip;

Determining a data access situation of the debug card and performing counting;

Setting an amount of data to be accessed each time; and

Ending the idle status; and If the data control chip is not in the idle status, accessing to the PCI bus data stored in the debug card according to the settings of the data control chip.

Cypress teaches: the step of controlling the access to the data stored in the buffer of debug card comprising: initializing the data control chip (Figure 2 illustrates the interface between a device and General Programmable Interface (GPIF), and the configuration sequence that ensues using the GPIFTool utility, page 3;

If the data control chip is in the idle status, setting the data control chip, wherein the setting step further comprises:

Setting a data access mode of the data control chip (The device via the interface is checked to see its idle status, page 3, paragraph 8);

Determining a data access situation of the debug card and performing counting (Peripheral FIFO write example of page 4 illustrates said function, which comprises counting);

Setting an amount of data to be accessed each time (Setting peripheral single write register, page 4); and

Ending the idle status (Routine 1 on page 8 illustrates ending the idle status, page 8); and If the data control chip is not in the idle status, accessing to the PCI bus data stored in the debug card according to the settings of the data control chip (Read transaction as illustrated in routine 2, page 8).

With regards to the applicant's argument on claim 8, the arguments presented do not comply with the requirements of 35 U.S.C.FR 1.111B, which states

In order to be entitled to reconsideration or further examination, the applicant or patent owner must reply to the Office action. The reply by the applicant or patent owner must be reduced to a writing which distinctly and specifically points out the supposed errors in the examiner's action and must reply to every ground of objection and rejection in the prior Office action. The reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references. If the reply is with respect to an application, a request may be made that objections or requirements as to form not necessary to further consideration of the claims be held in abeyance until allowable subject matter is indicated. The applicant's or patent owner's reply must appear throughout to be

a bona fide attempt to advance the application or the reexamination proceeding to final action. A general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references does not comply with the requirements of this section.

The applicant's response fail to present how the claim elements are distinguishable over the prior art applied. In addition, the language of the claim recites that the interface is operable, which merely means capable of, which does not expressly comprise the function.

However, the examiner has considered the arguments as a bona fide response. With regards to the applicant's argument that prior art does to meet the claimed limitation, the examiner points to the following teachings of Wu.

a debug card device, comprising: a PCI interface operable as a connecting interface with a PCI bus (Figure 2, PCI master element 111);

a storage module for storing PCI bus data; and

a data control chip operable to control the access and transmission of PCI bus data, the data control chip including: an access control module for controlling data access according to a control signal (SMB slave controller 112);

a transmission control module for controlling data transmission according to a control signal (SMB slave controller 112);

a data storage module for storing PCI bus data obtained from the debug card (PCI register block 20);

a register for storing an access control command (SMB slave controller 112 comprises said register); and

a host interface operable as an interface with a host (SMBUS interface 114).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAD
5/11/2007

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